UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/678,142	10/03/2000	Noriaki Sakamoto	10417-049001	6940

26211 7590 06/19/2006
FISH & RICHARDSON P.C.
P.O. BOX 1022
MINNEAPOLIS, MN 55440-1022

EXAMINER	
NORRIS, JEREMY C	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 06/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	09/678,142	SAKAMOTO ET AL.	
	Examiner	Art Unit	
	Jeremy C. Norris	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6,8,16,18,38,40,45,46,49,50,54,55,58,64 and 5962* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6,16,38 and 62* is/are allowed.

6)☒ Claim(s) *8,18,40,45,46,49,50,54,55,58 and 59* is/are rejected.

7)☒ Claim(s) *64* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

The indicated allowability of claims 8, 18, 40, 45, 46, 49, 50, 54, 55, 58, and 59 is withdrawn in view of the newly discovered reference(s) to US 5,702,567 and US 5,841,183. Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 8, 18, and 40 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 8, 18, and 40 state the limitation "wherein the conductive coating film is disposed on the second planar surface to form a passive element die pad and/or outer lead electrode, wherein a passive element to be place on the die pad comprises a chip resistor or a chip capacitor". However, since the claimed die pad is an optional feature it is unclear as to whether the chip resistor/capacitor must exist in occasion when the conductive coating film forms an outer lead electrode. For Examination purposes, the Examiner assumes that the outer lead electrode alternative is superfluous and has been treated as non-existent.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 8, 18, and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,221,428 (Ohsawa) in view of US 5,442,228 (Pham) and US 5,841,183 (Ariyoshi).

Ohsawa discloses a sheet-like board member (2) comprising: a first planar surface; a second planar surface disposed opposite to the first surface, said second planar surface having a semiconductor element mount region (8) defined thereon; and a

mask (9) disposed on the second planar surface and having a pattern corresponding to a plurality of first pads formed in or in the vicinity of the semiconductor element mount region, said mask comprising a conductive film, and guide holes (6) into which guide pins are inserted (10). Ohsawa does not specifically state that one unit comprises a plurality of die pads. However, it is well known in the art to provide multiple die pads on a leadframe for the purpose of packaging multiple devices together as evidenced by Pham (figure 2, col. 2, lines 20-35). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to provide multiple die pas in a unit in the invention of Ohsawa as is known in the art and evidenced by Pham. The motivation for doing so would have been to effectively package multiple devices together thus reducing required mounting space. The modified invention of Ohsawa additionally teaches wherein the conductive coating film is disposed on the second planar surface to form a passive element die pad and/or outer lead electrode. However the modified invention of Ohsawa does not specifically teach that the passive element to be place on the die pad comprises a chip resistor or a chip capacitor [claim 8]. However, it is well known in the art to mount chip resistors on die pads of lead frames as evidenced by Ariyoshi (col. 1, lines 5-10). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use a chip resistor as the passive element in the modified invention of Ohsawa as is known in the art and evidenced by Ariyoshi. The motivation for doing so would have been to provide circuit conditioning via the resistor to the device.

Similarly, Ohsawa discloses, a sheet-like board member (2) comprising: a first planar surface; a second planar surface disposed opposite to the first planar surface; a protuberance formed on said second planar surface; and guide holes (6) into which guide pins are inserted, wherein the protuberance comprises a plurality of first pads (8) in or in the vicinity of a semiconductor element mount region defined on the second planar surface. Ohsawa does not specifically state that one unit comprises a plurality of die pads. However, it is well known in the art to provide multiple die pads on a leadframe for the purpose of packaging multiple devices together as evidenced by Pham (figure 2, col. 2, lines 20-35). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to provide multiple die pas in a unit in the invention of Ohsawa as is known in the art and evidenced by Pham. The motivation for doing so would have been to effectively package multiple devices together thus reducing required mounting space. The modified invention of Ohsawa additionally teaches, wherein the protuberance comprises passive element die pads and/or outer lead electrodes. However the modified invention of Ohsawa does not specifically teach that the passive element to be place on the die pad comprises a chip resistor or a chip capacitor [claim 18]. However, it is well known in the art to mount chip resistors on die pads of lead frames as evidenced by Ariyoshi (col. 1, lines 5-10). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use a chip resistor as the passive element in the modified invention of Ohsawa as is known in the art and evidenced by Ariyoshi. The motivation for doing so would have been to provide circuit conditioning via the resistor to the device.

Moreover Ohsawa discloses a sheet-like board member (2) comprising: a first planar surface a second planar surface disposed opposite to the first surface, said second planar surface having a semiconductor element mount region defined thereon; and a mask (9 or alternately 5a) for etching disposed on the second planar surface and having a pattern corresponding to a plurality of first pads (8) formed in or in the vicinity of the semiconductor element mount region and guide holes into which guide pins are inserted. Ohsawa does not specifically state that one unit comprises a plurality of die pads. However, it is well known in the art to provide multiple die pads on a leadframe for the purpose of packaging multiple devices together as evidenced by Pham (figure 2, col. 2, lines 20-35). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to provide multiple die pas in a unit in the invention of Ohsawa as is known in the art and evidenced by Pham. The motivation for doing so would have been to effectively package multiple devices together thus reducing required mounting space. The modified invention of Ohsawa additionally teaches, wherein the conductive coating film is disposed on the second planar surface to form a passive element die pad and/or outer lead electrode. However the modified invention of Ohsawa does not specifically teach that the passive element to be place on the die pad comprises a chip resistor or a chip capacitor [claim 40]. However, it is well known in the art to mount chip resistors on die pads of lead frames as evidenced by Ariyoshi (col. 1, lines 5-10). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use a chip resistor as the passive element in the modified invention of Ohsawa as is known in the art and evidenced by Ariyoshi. The motivation

for doing so would have been to provide circuit conditioning via the resistor to the device.

Claims 45, 46, 49, 50, 54, 55, 58 and 59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohsawa in view of Pham and US 5,702,567 (Mitsui).

Ohsawa discloses a sheet-like board member (2) comprising: a first planar surface; a second planar surface disposed opposite to the first surface, said second planar surface having a semiconductor element mount region (8) defined thereon; and a mask (9) disposed on the second planar surface and having a pattern corresponding to a plurality of first pads formed in or in the vicinity of the semiconductor element mount region, said mask comprising a conductive film, and guide holes (6) into which guide pins are inserted (10). Ohsawa does not specifically state that one unit comprises a plurality of die pads. However, it is well known in the art to provide multiple die pads on a leadframe for the purpose of packaging multiple devices together as evidenced by Pham (figure 2, col. 2, lines 20-35). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to provide multiple die pas in a unit in the invention of Ohsawa as is known in the art and evidenced by Pham. The motivation for doing so would have been to effectively package multiple devices together thus reducing required mounting space. The modified invention of Ohsawa does not specifically teach that a positioning mark is provided on the sheet-like board member [claim 45], wherein the positioning mark is formed by partially etching the sheet-like board member [claim 46]. However, Mitsui teaches forming a positioning

mark by etching a substrate (col. 1, lines 60-65). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form a positioning mark in the board of the modified invention of Ohsawa by etching as taught by Mitsui. The motivation for doing so would have been to provide a reference for alignment that is formed simultaneously with other features (Mitsui col. 1, line 60 – col. 2, line 10).

Similarly, Ohsawa discloses, a sheet-like board member (2) comprising: a first planar surface; a second planar surface disposed opposite to the first planar surface; a protuberance formed on said second planar surface; and guide holes (6) into which guide pins are inserted, wherein the protuberance comprises a plurality of first pads (8) in or in the vicinity of a semiconductor element mount region defined on the second planar surface. Ohsawa does not specifically state that one unit comprises a plurality of die pads. However, it is well known in the art to provide multiple die pads on a leadframe for the purpose of packaging multiple devices together as evidenced by Pham (figure 2, col. 2, lines 20-35). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to provide multiple die pas in a unit in the invention of Ohsawa as is known in the art and evidenced by Pham. The motivation for doing so would have been to effectively package multiple devices together thus reducing required mounting space. The modified invention of Ohsawa does not specifically teach that a positioning mark is provided on the sheet-like board member [claim 49], wherein the positioning mark is formed by partially etching the sheet-like board member [claim 50]. However, Mitsui teaches forming a positioning mark by etching a substrate (col. 1, lines 60-65). Therefore, it would have been obvious

to one having ordinary skill in the art at the time of invention to form a positioning mark in the board of the modified invention of Ohsawa by etching as taught by Mitsui. The motivation for doing so would have been to provide a reference for alignment that is formed simultaneously with other features (Mitsui col. 1, line 60 – col. 2, line 10).

Additionally, Ohsawa, discloses, a sheet-like board member (2) comprising: a planar surface; a sheet-like front side of predetermined thickness which is provided on the planar surface; a plurality of first pads (8) formed in or in the vicinity of a semiconductor element mount region defined on the planar surface; protuberances formed on said planar surface and include wirings (fig. 2B) integrally formed with the first pads, said plurality of first pads and said protuberances formed within an abutting region defined on said planar surface and guide holes (6) into which guide pins are inserted. Ohsawa does not specifically state that one unit comprises a plurality of die pads. However, it is well known in the art to provide multiple die pads on a leadframe for the purpose of packaging multiple devices together as evidenced by Pham (figure 2, col. 2, lines 20-35). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to provide multiple die pas in a unit in the invention of Ohsawa as is known in the art and evidenced by Pham. The motivation for doing so would have been to effectively package multiple devices together thus reducing required mounting space. The modified invention of Ohsawa does not specifically teach that a positioning mark is provided on the sheet-like board member [claim 54], wherein the positioning mark is formed by partially etching the sheet-like board member [claim 55]. However, Mitsui teaches forming a positioning mark by etching a substrate (col. 1,

lines 60-65). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form a positioning mark in the board of the modified invention of Ohsawa by etching as taught by Mitsui. The motivation for doing so would have been to provide a reference for alignment that is formed simultaneously with other features (Mitsui col. 1, line 60 – col. 2, line 10).

Examiner notes that the limitation "said abutting region provided to contact with an upper metal mold" [claim 54] is an intended use limitation and is thus only considered to the extent that the limitation impacts the claimed structure. Thus a prior art meeting all the other claimed structural limitations only needs to be capable of being used in the claimed manner.

Moreover Ohsawa discloses a sheet-like board member (2) comprising: a first planar surface a second planar surface disposed opposite to the first surface, said second planar surface having a semiconductor element mount region defined thereon; and a mask (9 or alternately 5a) for etching disposed on the second planar surface and having a pattern corresponding to a plurality of first pads (8) formed in or in the vicinity of the semiconductor element mount region and guide holes into which guide pins are inserted. Ohsawa does not specifically state that one unit comprises a plurality of die pads. However, it is well known in the art to provide multiple die pads on a leadframe for the purpose of packaging multiple devices together as evidenced by Pham (figure 2, col. 2, lines 20-35). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to provide multiple die pas in a unit in the invention of Ohsawa as is known in the art and evidenced by Pham. The motivation for doing so

would have been to effectively package multiple devices together thus reducing required mounting space. The modified invention of Ohsawa does not specifically teach that a positioning mark is provided on the sheet-like board member [claim 58], wherein the positioning mark is formed by partially etching the sheet-like board member [claim 59]. However, Mitsui teaches forming a positioning mark by etching a substrate (col. 1, lines 60-65). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form a positioning mark in the board of the modified invention of Ohsawa by etching as taught by Mitsui. The motivation for doing so would have been to provide a reference for alignment that is formed simultaneously with other features (Mitsui col. 1, line 60 – col. 2, line 10).

Allowable Subject Matter

Claims 6, 16, 38, and 62 are allowed.

Claim 64 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments with respect to claims 8, 18, 40, 45, 46, 49, 50, 54, 55, 58, and 59 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeremy C. Norris whose telephone number is 571-272-1932. The examiner can normally be reached on Monday - Friday, 9:30 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JCSN

Jeremy C. Norris
Patent Examiner
Technology Center 2800